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reduce + power consumption + increase + cl

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The superior throughput of the AVR32 core **reduces** the number of **clock** cycles required and hence **reduces power consumption**. In addition, the AVR32 is ...

[www.atmel.com/dyn/corporate/view_detail.asp?ref=&](http://www.atmel.com/dyn/corporate/view_detail.asp?ref=&FileName=AVR32bit_long_2_14.html&SEC_NAME=Product)

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AnandTech: Intel's Pentium Extreme Edition 965: The Last of a ...

With no **clock** signal, none of the logic in the chip will do anything and thus **power consumption is reduced**. Performance is also significantly **reduced**; ...

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BDTI - Low Power Programmable DSPs

A **clock** divider **reduces** the processor's **clock** rate by a programmable factor. This in turn **reduces** the processor's execution rate and **power consumption**. ...

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Inside DSP | Inside DSP on Low Power: Designing Low-Power Signal ...

In addition, **clock** frequencies are continually increasing in order to satisfy ...

Reducing System Power Consumption Perhaps the most effective technique for ...

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power consumption. **Reducing clock** frequency alone doesn't necessarily **reduce power**, ... A common approach to **power reduction** is to first **increase** ...

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Energy-Efficient System Architecture Aims to Improve System Energy ...

... slowing the **clock** rate for some components to **increase power** conversion

efficiency. Slowing the **clock** **reduces** the **power consumed** in the CMOS circuits, ...

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Intel386™ Processors - Overview

Powerdown disables the **clock** to both the CPU core and peripherals. In this mode, current **consumption** is **reduced** to a few microamps. The **power** management ...

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microprocessors is to **reduce** supply voltage and **clock** ... tural features which **reduce power consumption** do not. **increase** execution latency so much that ...

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CSAIL Research Abstract

But the time slack obtained from pipelining can also be used to **reduce power consumption** by lowering supply voltage at a fixed **clock** frequency (Figure 2). ...